WHAT IS CLAIMED IS:

1. An information processing apparatus, comprising:

a clock generator for generating a clock,

a clock controller for controlling the clock generated by the clock generator to determine a clock frequency,

a storage for storing a software,

a computing device for implementing the software obtained from the storage in accordance with the clock supplied via the clock controller,

a specific processing section detector for detecting the start and end of a specific processing section which is a section during which a predetermined specific processing is executed, and

a clock control judging device for outputting a command to control the clock frequency to the clock controller in accordance with a result obtained by the specific processing section detector,

wherein the clock control judging device commands the clock controller to increase the clock frequency if the specific processing section detector has detected the start of the specific processing section while commanding the clock controller to decrease the clock frequency if the specific processing section detector has detected the end of the specific processing section.

2. An information processing apparatus according to claim 1, wherein the specific processing section is a section during which an exclusive processing is executed.

3. An information processing apparatus according to claim 1, wherein the specific processing section is a predetermined specific section

out of a plurality of sections during which exclusive processings are executed.

4. An information processing apparatus according to claim 1, further comprising a power-source controller for controlling a voltage to be supplied to the computing device and the storage upon obtaining clock frequency information from the clock controller, wherein the power-source controller increases the voltage when the clock frequency is increased while decreasing the voltage when the clock frequency is decreased.

5. An information processing apparatus according to claim 4, wherein the clock controller increases the clock frequency in a stepwise manner within a range where the computing device is operable as the voltage is increased by the power-source controller.

6. An information processing apparatus according to claim 4, wherein the clock control judging device:

predicts a specific processing time, which is a time up to the end of the specific processing section, based on a time required for a previous specific processing if the specific processing section detector has detected the start of the specific processing section,

notifies a command to increase the clock frequency to the clock controller when the predicted specific processing time exceeds a threshold value, and

does not notify the command to increase the clock frequency to the clock controller when the predicted specific processing time is below the threshold value.

7. An information processing apparatus according to claim 6,

wherein the clock control judging device sets a time dependent on and equal to or longer than a voltage-increasing time required for the power-source controller to increase the voltage as the threshold value.

8. An information processing apparatus according to claim 7, wherein the clock control judging device sets a time dependent on and equal to or longer than a sum of the voltage-increasing time and a voltage-decreasing time required for the power-source controller to decrease the voltage as the threshold value.

9. An information processing apparatus according to claim 6, wherein the clock control judging device sets a time dependent on and equal to or longer than a frequency-increasing time required for the clock controller to increase the clock frequency as the threshold value.

10. An information processing apparatus according to claim 9, wherein the clock control judging device sets a time dependent on and equal to or longer than a sum of the frequency-increasing time and a frequency-decreasing time required for the clock controller to decrease the clock frequency as the threshold value.

11. An information processing apparatus according to claim 4, wherein the clock control judging device:

predicts a low-speed specific processing time which is a time up to the end of the specific processing section when the clock frequency is kept low and a high-speed specific processing time which is a time up to the end of the specific processing section when the clock frequency is increased, based on a time required for a previous specific processing if the specific processing section detector has detected the start of the specific processing

section, and

notifies a command to increase the clock frequency to the clock controller when the predicted low-speed specific processing time exceeds a threshold value dependent on and equal to or longer than a sum of the predicted high-speed specific processing time and a voltage-changing time required for the power-source controller to increase and decrease the voltage,

and does not notify the command to increase the clock frequency to the clock controller when the predicted low-speed specific processing time is below the threshold value.

12. An information processing apparatus according to claim 4, wherein the clock control judging device:

predicts a low-speed specific processing time which is a time up to the end of the specific processing section when the clock frequency is kept low and a high-speed specific processing time which is a time up to the end of the specific processing section when the clock frequency is increased, based on a time required for a previous specific processing if the specific processing section detector has detected the start of the specific processing section, and

notifies a command to increase the clock frequency to the clock controller when the predicted low-speed specific processing time exceeds a threshold value dependent on and equal to or longer than a sum of the predicted high-speed specific processing time and a frequency-changing time required for the clock controller to increase and decrease the clock frequency,

and does not notify the command to increase the clock frequency to the clock controller when the predicted low-speed specific processing time is below the threshold value.

13. An information processing apparatus according to claim 4, wherein the clock control judging device:

predicts a high-speed specific processing time, which is a time up to the end of the specific processing section when the clock frequency is increased within a predetermined range, and a low-speed specific processing time, which is a time up to the end of the specific processing section when the clock frequency is kept low, based on a time required for a previous processing if the specific processing section detector has detected the start of the specific processing section,

notifies a command to increase the clock frequency to an effective frequency to the clock controller when the effective frequency, at which the predicted low-speed specific processing time is longer than a threshold value dependent on and equal to or longer than a sum of the predicted high-speed specific processing time and a voltage-changing time required for the power-source controller to increase and decrease the voltage, lies within the predetermined range,

and does not notify the command to increase the clock frequency to the clock controller when the effective frequency lies beyond the predetermined range.

14. An information processing apparatus according to claim 13, wherein the clock control judging device, if a plurality of frequencies as the effective frequency lie within the predetermined range, then notifies a

command to increase the clock frequency up to the highest one of the plurality of frequencies to the clock controller.

15. An information processing apparatus according to claim 4, wherein the clock control judging device:

predicts a high-speed specific processing time, which is a time up to the end of the specific processing section when the clock frequency is increased within a predetermined range, and a low-speed specific processing time, which is a time up to the end of the specific processing section when the clock frequency is kept low, based on a time required for a previous processing if the specific processing section detector has detected the start of the specific processing section,

notifies a command to increase the clock frequency to an effective frequency to the clock controller when the effective frequency, at which the predicted low-speed specific processing time is longer than a threshold value dependent on and equal to or longer than a sum of the predicted high-speed specific processing time and a frequency-changing time required for the clock controller to increase and decrease the clock frequency, lies within the predetermined range, and

does not notify the command to increase the clock frequency to the clock controller when the effective frequency lies beyond the predetermined range.

16. An information processing apparatus according to claim 4, wherein the clock control judging device:

predicts a low-speed nonspecific processing time, which is a time up to the next detection of the start of the specific processing section when the

clock frequency is decreased, based on a time required for a previous processing if the specific processing section detector has detected the end of the specific processing time, and

notifies a command to decrease the clock frequency to the clock controller when the predicted low-speed nonspecific processing time exceeds a threshold value and does not notify the command to decrease the clock frequency to the clock controller when the predicted low-speed nonspecific processing time is below the threshold value.

17. An information processing apparatus according to claim 16, wherein the clock control judging device sets a time dependent on and equal to or longer than a voltage-decreasing time required for the power-source controller to decrease the voltage as the threshold value.

18. An information processing apparatus according to claim 17, wherein the clock control judging device sets a time dependent on and equal to or longer than a sum of the voltage-decreasing time and a voltage-increasing time required for the power-source controller to increase the voltage as the threshold value.

19. An information processing apparatus according to claim 16, wherein the clock control judging device sets a time dependent on and equal to or longer than a frequency-decreasing time required for the clock controller to decrease the clock frequency as the threshold value.

20. An information processing apparatus according to claim 19, wherein the clock control judging device sets a time dependent on and equal to or longer than a sum of the frequency-decreasing time and a frequency-increasing time required for the clock controller to increase the clock

frequency as the threshold value.

21. An information processing apparatus according to claim 4, wherein the clock control judging device:

predicts a low-speed nonspecific processing time, which is a time up to the start of the next specific processing section when the clock frequency is decreased within a predetermined range, based on a time required for a previous processing other than the specific processing if the specific processing section detector has detected the end of the specific processing section,

notifies a command to decrease the clock frequency to an effective frequency to the clock controller when the effective frequency, at which the predicted low-speed nonspecific processing time is longer than a threshold value dependent on and equal to or longer than a voltage-changing time required for the power-source controller to decrease and increase the voltage, lies within the predetermined range, and

does not notify the command to decrease the clock frequency to the clock controller when the effective frequency lies beyond the predetermined range.

22. An information processing apparatus according to claim 21, wherein the clock control judging device, if a plurality of frequencies as the effective frequency lie within the predetermined range, then notifies a command to decrease the clock frequency down to the lowest one of the plurality of frequencies to the clock controller.

23. An information processing apparatus according to claim 4, wherein the clock control judging device:

predicts a low-speed nonspecific processing time, which is a time up to the start of the next specific processing section when the clock frequency is decreased within a predetermined range, based on a time required for a previous processing other than the specific processing if the specific processing section detector has detected the end of the specific processing section,

notifies a command to decrease the clock frequency to an effective frequency to the clock controller when the effective frequency, at which the predicted low-speed nonspecific processing time is longer than a threshold value dependent on and equal to or longer than a frequency-changing time required for the clock controller to decrease and increase the clock frequency, lies within the predetermined range, and

does not notify the command to decrease the clock frequency to the clock controller when the effective frequency lies beyond the predetermined range.

24. An electrical apparatus comprising an information processing apparatus, comprising:

a clock generator for generating a clock,

a clock controller for controlling the clock generated by the clock generator to determine a clock frequency,

a storage for storing a software,

a computing device for implementing the software obtained from the storage in accordance with the clock supplied via the clock controller,

a specific processing section detector for detecting the start and end of a specific processing section which is a section during which a

predetermined specific processing is executed, and

a clock control judging device for outputting a command to control the clock frequency to the clock controller in accordance with a result obtained by the specific processing section detector,

wherein the clock control judging device commands the clock controller to increase the clock frequency if the specific processing section detector has detected the start of the specific processing section while commanding the clock controller to decrease the clock frequency if the specific processing section detector has detected the end of the specific processing section.

25. A clock controlling method for an information processing apparatus, comprising:

a specific processing section detecting step of detecting the start and end of a specific processing section which is a section during which a predetermined specific processing is executed, and

a clock controlling step of increasing a clock frequency of the information processing apparatus when the start of the specific processing section is detected in the specific processing section detecting step while decreasing the clock frequency when the end of the specific processing section is detected in the specific processing section detecting step.

26. A clock controlling program for causing an information processing apparatus to realize:

a specific processing section detecting function of detecting the start and end of a specific processing section which is a section during which a predetermined specific processing is executed, and

a clock controlling function of increasing a clock frequency of the information processing apparatus when the start of the specific processing section is detected in the specific processing section detecting function while decreasing the clock frequency when the end of the specific processing section is detected in the specific processing section detecting function.

27. A program product, comprising:

a clock controlling program for causing an information processing apparatus to realize:

a specific processing section detecting function of detecting the start and end of a specific processing section which is a section during which a predetermined specific processing is executed, and

a clock controlling function of increasing a clock frequency of the information processing apparatus when the start of the specific processing section is detected in the specific processing section detecting function while decreasing the clock frequency when the end of the specific processing section is detected in the specific processing section detecting function, and

a signal holding medium for holding the program.

28. A program product according to claim 27, wherein the signal holding medium is at least one of a storage medium and a transmission medium.